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Implementation Of One bit Parallel Memory Cell using Quatum Dot Cellular Automata

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Abstract: *The Integrated Circuit Technology(IC) is growing day by day to improve circuit performance. Quantum dot cellular automata (QCA) is one of the noval technology in nano electronics, introduced to overcome the scaling limitations takes place in CMOS Technology. This technology is suitable for development of ultra-dense low-power high-performance digital circuits. In this paper we are implementing a 2:1 multiplexer using QCA followed by its application in the designing of a 1-bit parallel memory cell. A multiplexer is an effective element for the design of many significant circuits. All the drawbacks of CMOS technology should be improved by QCA technology, as there is no power loss and temperature effect. Using cascade connection of two 2:1 multiplexers, we are designing a 4:1 multiplexer. The simulation can be done and verified using QCA designer software.*

Keywords*: Quantum Dot Cellular Automata, Clock zone, Majority Gate, Multiplexer, and Parallel Memory.*

I. Introduction

According to Gordon Moore(1965), the number of transistors that can be integrated on to a single chip will double every 18 months. This law put forth by Moore has been a benchmark for semiconductor scaling. The IC industry which has been primarily driven by CMOS technology scaling is now forced to look into other alternatives as the scaling is fast approaching its fundamental limits. The VLSI industry needs the circuits with high packing density, less power, low cost and high speed digital circuits.CMOS technology having certain limitations like the scaling of the MOSFET, switching power and speed. Therefore, to overcome the limitations of CMOS technology, we needs new technologies has to be implementing. QCA is one of the new emerging nano technology. QCA is a new technique, which can be used at nanoscale to design digital circuits. At present QCA can be

Considered as the most outstanding substitute for CMOS technology, as there is no power loss and temperature effect. There are several advantages of this technology like [1] -1.The speed of operation is very high, 2.Power consumption is low, 3. Device density is high.The multiplexer is a combinational circuit, which permits picking one output amid numerous inputs. It transfers one of the inputs to the output at a time, so it is also known as Data selector. This type of operation facilitates to share one costly device for more than one application in a system. Due to its abundant use, it has become necessary to implement a multiplexer circuit, which is area efficient, which results in the reduction of the cost of designing. Till now various QCA based Multiplexers have been designed [2] to [6]. QCA structures are mostly designed using coplanar wire crossing. However, this type of wire crossing is enormously prone to external effects as well as crosstalk [7].In [8] a successful attempt is reported to design a multiplexer circuit without using coplanar wire crossing. In [9], three clock zones based approach is used to design a modular multiplexer. In this paper also, a modular 2:1 MUX and using that 2:1 MUX a 4:1 MUX is also designed. By cascading of this 2:1 MUX, any higher order MUX can be designed.

1. QCA Back Ground

The principle of Quantum Dot Cellular was first proposed by Lent et al. in the year 1993 [10]. Craig Lent and Doug proposed implementations of systems based on classical cellular automata designed using quantum dots as a replacement for the classical computation using CMOS. In order to differentiate this proposal and the models of cellular automata which are used for performing quantum computation, many authors refers to this subject as Quantum-dot Cellular Automata (QCA). QCA is a novel emerging technology in which logic states are not stored as voltage levels, but rather the position of the individual electron [1]. In QCA, binary information is represented by bi-stable charge configuration. The fundamental unit of Quantum Dot Cellular Automata is QCA Cell. A QCA cell is shown in Fig 1. Each QCA cell contains four quantum dots at the corner of the cell and electrons reside in two of the Quantum Dots. Electrons reside at diagonally opposite quantum dots, because at that position, Coulomb repulsion force is least. Polarization P measures the extent to which the

charge distribution is aligned along one of the diagonal axes. If the charge density on a dot is then the polarization is defined in (1) [11] [12]:

$$P = \frac{(p1+p3)-(p2+p4)}{p1+p2+p3+p4} \qquad (1)$$

1.1 POLARIZATION STATE

In QCA, logic states are represented by two possible charge configurations. A basic QCA Cell is shown in Fig. 1. Based on position of electrons in QCA cell there are two types of polarization states exist. QCA cells representing Logic 0 and Logic 1 are shown in Fig. 2(a) and 2(b) respectively. Cell representing logic 0 has polarization P = -1 and cell representing logic 1 has polarization P = +1.

1.2 Majority Gate

The Coulomb collaboration force between the cells partners the condition of one cell to the condition of neighbor cells. Because of this communication, neighboring cells organize their polarization. The ancient logic gate in QCA is Majority Logic Gate.. It comprises of 5 QCA cells, arranged in a plus sign manner as shown in Fig. 3. It has three inputs, one output, and a driver cell. The logic function of Majority gate is shown in (2).

$$Maj(A,B,C) = AB + BC + CA \qquad (2)$$

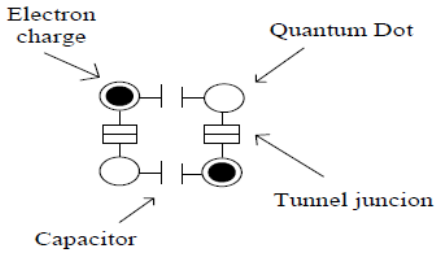


Fig.1. A QCA Cell

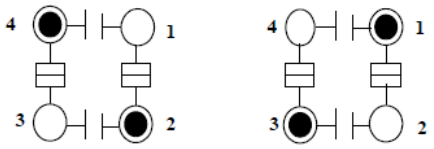


Fig 2. Tunnling Effect

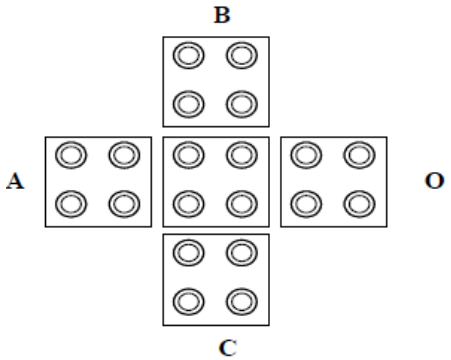


Fig 3.QCA Majority gate

Functioning of AND Gate and OR Gate can be obtained from this Majority gate by setting one of the input to logic 0 and logic 1 as shown in Fig 4 (a) and (b) respectively. In addition to this, Not Gate functioning is obtained by using QCA inverter circuit as shown in Fig 5. All digital circuit can be designed using these two logic primitives.In QCA, information transmits from one place to another in QCA binary wires. QCA binary wires are constructed from an array of cells having the same polarization as shown in Fig 6.

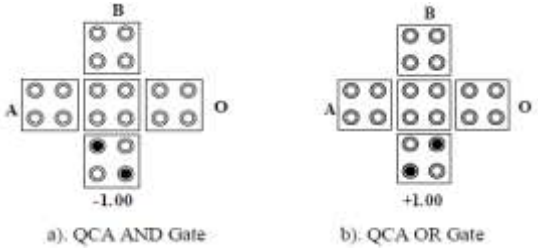


Fig 4. Logic gates

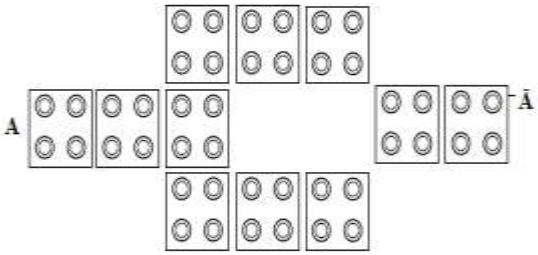


Fig.5. Inverter

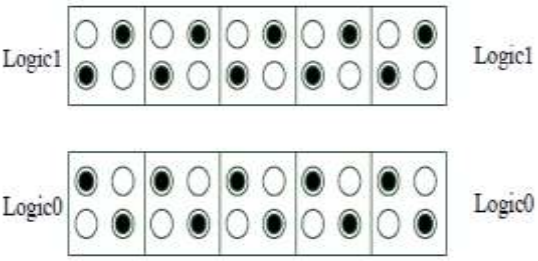


Fig.6. Binary wire

1.3 QCA Clock

Clocking of QCA is suggested in [13]. In QCA, clocking is a crucial parameter; it is used for providing power to the circuit and also for controlling the flow of information. The clock signal is generated by the application of an electric field to the cell, which raises or lowers the tunneling barrier between the quantum dots in the cell which enables the transfer of electrons between the cells. Clocking (by application of an appropriate voltage to a cell) leads to adjustment of tunneling barriers between quantum dots for transfer of electrons between the dots [14]. In QCA, clocking is accomplished by two techniques: zone clocking and continuous clocking. In Zone Clocking [15], each clock has four clock phases are used: switch, hold, release and relax as shown in Fig. 7. Color coding for different cells is shown in Fig. 8.

Switch phase-In the beginning, cells remain in the unpolarized state and have low potential barriers, then barriers are raised.

Hold phase- In this phase, potential barriers are kept high.

Release phase-In this phase, potential barriers are brought down.

Relax phase-In this phase potential barrier of the cells kept at low state and cells remain in the unpolarized state.

In Continuous clocking, potential field is generated by the system of submerged electrodes

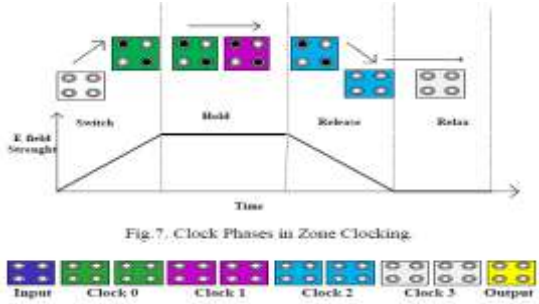


Fig.7. Clock Phases in Zone Clocking

Fig.8 colour coding of clocks in zone clocking

II. Previous Work

In [2] Kyosun Kim et al. have analyzed the causes of the failure of QCA circuits and have proposed an adder circuit, which utilizes a multiplexer. Proper clocking scheme is exploited in this design. They have told that the state of a multiple input QCA design depends on all the inputs, which result in a variety of sneak noise paths in QCA. So they systematically analyzed the sneak noise paths in QCA- based design by using the concept of kink energy. In addition, this analysis is significant due to its influence as the design size grows. They have also analyzed the failure of majority gates, and then they used the coplanar clocking technique in the design of full adder to overcome the errors. The multiplexer, which has been used by them, uses clock gating which is faster and smaller.

In [3] Mardirisi and Karafyllidis have proposed modular to 1 multiplexer which is formulated to increase the circuit stability. They have used the concept of crossover design for signal propagation and have shown each logic gate with a block. Each block consists of two pairs of cells serially connected which produces signal delay equal to the number of included cell pairs. Their proposed design of 2:1 MUX consists of 56 cells and area is about 0.07μ . They have also shown a 4:1 MUX which consists of 215 cells covering an area of inputs is 6 clock phases i.e. 1.5 clock cycles.In [4] Hashemi et al. have proposed multiplexer in three layers in which the first layer is the backbone of the circuit.

This new design is denser with four clocks latency and faster. Also a 4:1MUX has shown 33% improvement in reducing complexity and 28% improvement in the area. The proposed structure is reliable at high frequency when the number of inputs becomes larger.

In [5] Roohi et al. have designed 2:1 multiplexer using three clock zones due to this delay have been increased. In [6] Sen et al. have proposed a modular design of 2:1 MUX that in turn used to synthesize 4:1 and 8:1 MUX. The design of 2:1 MUX is efficient as having less delay and involving only two clock zones. The improvement in 4:1 MUX and 8:1 MUX is about 27.9% and 27% respectively. They have done the power dissipation analysis of 8:1 MUX and shown that the circuit is energy efficient. They have also discussed fault tolerant behavior of the multiplexer circuits. For this purpose, they have used the HDLQ Verilog library to convert the QCA equivalent in hardware description language. Their proposed design produces an average of 77.62% correct outputs even when the design is faulty.

Although many researchers have done remarkable work in the field of design of multiplexers but still the circuit is not competent with the current trend of area constraint. And this force to think and develop an efficient design of 2:1 MUX, which can be further used to design any complex logic. And thus in this paper the proposed design of 2:1 MUX is proved to be efficient regarding the number of cells consumed, and the area required. Also the power dissipation analysis of the 4:1 MUX is done to check the power consumption of the design.

III. Proposed Work

The multiplexer is an essential digital circuit. It has many applications like it is used in the design of memory and FPGA circuits and it can also be used to implement many Boolean functions. It has inputs, one output and n select lines, which transfers one of input to the output based on the value of the select lines. Many eminent researchers have shown the structure of multiplexer and gave valid statements regarding its benefits. The proposed design of multiplexer in [6] uses only two zones of clocking scheme i.e. clock 0 and clock 1. Based on similar approach, here two different designs of 2:1 MUX have been proposed. Moreover, the proposed structure is competent as well as powerful in terms of number of cells used to design the circuit. multiplexer in terms of number of cells used and area occupied by the design.

1.4 2:1 MUX

The conventional circuit of 2:1 MUX has two Data inputs I0 and I1, one select line S and one output Out. The truth table is given in Table 1, and the block diagram is shown in Fig. 9. The Logic function of Output O is given in (3).

$$O = I0\bar{S} + I1S \qquad (3)$$

Table1.Truth table 2:1 MUX

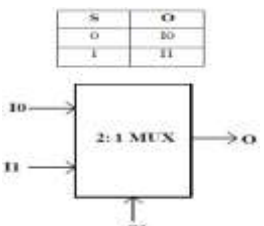


Fig.9. Graphical symbol of 2:1 MUX

The output equation reveals that the MUX can be implemented using two AND gates, one NOT Gate and one OR Gate. One inverter and three Majority Gates are required to design this MUX. The QCA equivalent block diagram and QCA layout is shown in Fig.10.and Fig.11 The majority based output expression of this circuit is given in (4).

$$O = Maj(Maj(I0, \bar{S}, 0), Maj(I1, S, 0)) \quad (4)$$

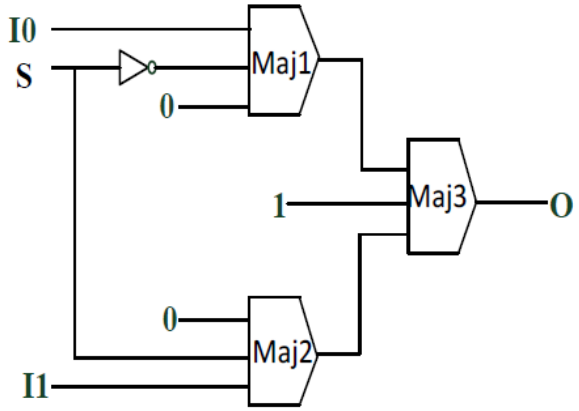


Fig.10. Schematic diagram of 2:1 MUX

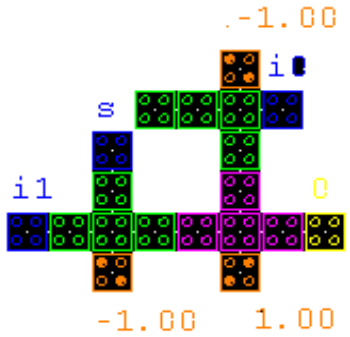


Fig.11.QCA Layout 2:1 MUX

The logic gates can be implemented using the 2:1 MUX can be seen from below .

Theorem1:A 2:1 MUX can be used to implement a two-input OR Gate.

Proof: Put select line S=X, inputs I0=Y and I1=1.Then 2:1 mux implements OR operations of inputs X and Y i.e. Out= X+Y.

Theorem 2- A 2:1 MUX can be used to implement a two-input AND Gate.

Proof: Put select line S =X, inputs I0=0 and I1=Y. Then 2:1 mux implements AND operation of inputs X and Y i.e. Out=X.Y.

Theorem 3- A 2:1 MUX can be used to implement 1 two input NAND gate.

Proof: Put select line S =X and Inputs I 0= 1 and I1=¯.Then 2:1 mux implements NAND operation of X and Y i.e. Out= $\overline{XY}$.

Theorem 4: A 2:1 MUX can be used to implement a two-input NOR gate.

Proof: Put select line S =X and inputs I 0=¯ and I1=0. Then 2:1 mux implements NOR operation of X and Y i.e. Out= $\overline{X+Y}$.

Theorem 5: A 2:1 MUX can be used to implement a two-input EXOR gate.

Proof: Put select line S =X and inputs I 0= Y and I 1=¯Then 2:1 MUX implements XOR operation of X and Y i.e. Out= $X \oplus Y$

Theorem 6: A 2:1 MUX can be used to implement a two-input XNOR gate.

Proof: Put select line S =X and inputs I 0=¯, Then 2:1mux implements XNOR operation of X and Y i.e. Out= X©Y

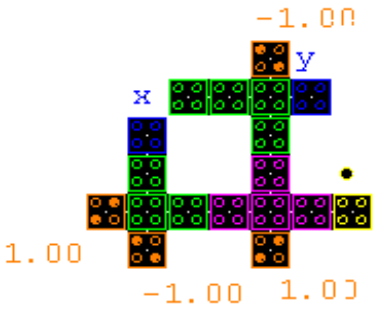


Fig .a. OR Gate

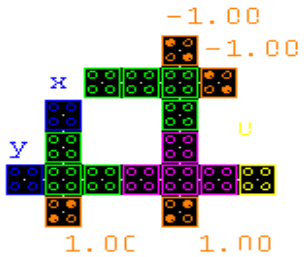


Fig .b. AND Gate

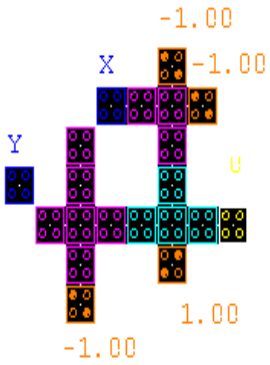


Fig .c. Nor Gate

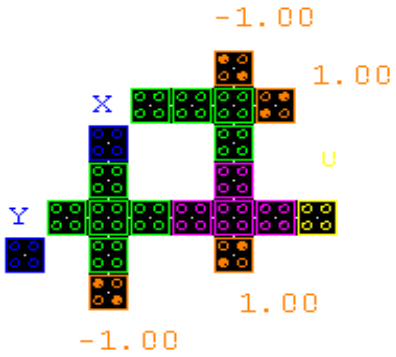


Fig .d .Nand Gate

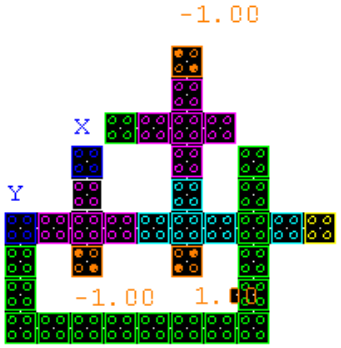


Fig .e. XOR Gate

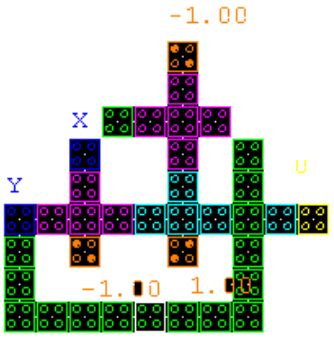


Fig .f. XNOR Gate

1.1 4:1 MUX

4:1 MUX has four data inputs I0, I1, I2 and I3, two select lines S0 and S1 and one output O. Output of this MUX is given in (5). Figures and Tables

$$Out = I0\overline{S1}\,\overline{S0} + I1\overline{S1}S0 + I2S1\overline{S0} + I3S1S0 \qquad (5)$$

Table 2. Truth Table of 4:1 MUX

S1	S0	OUT
0	0	I0
0	1	I1
1	0	I2
1	1	I3

If 4:1MUX is designed directly using (4), then it will require 15 majority gates. However, if some modification is done in the above equation, the same functionality can be obtained using only nine majority gates as shown in (6).

$$Out = I0\overline{S1}\,\overline{S0} + I1\overline{S1}S0 + I2S1\overline{S0} + I3S1S0$$

$$= \overline{S1}(I0\overline{S0} + I1S0 + S1(I2\overline{S0} + I3S0) \qquad (6)$$

Above output expression using majority logic is shown in (7).

$$Out = M(M(\overline{S1}, (M(I0, \overline{S0}, 0), M(I1, S0, 0)), 0), (M(\overline{S1}, (M(I0, \overline{S0}, 0), M(I1, S0, 0), 1)), 0), 1) \qquad (7)$$

The proposed 4:1 Mux has been designed by cascading three 2:1 Mux as shown in Fig 15.Its schematic and QCA layout is shown in Fig. 14 and Fig. 16 respectively. In this design clock zone based crossover [16] is used. This recently discovered clock zone based crossover is very robust and fast in operation and has very low cost as described in [17] and [18]. In this approach, the phase difference between two clock zones of the two crossed wires is 180 degrees.

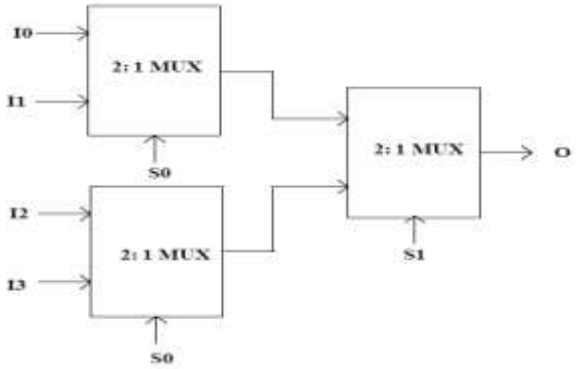


Fig.14.4:1MUX using 2:1MUX

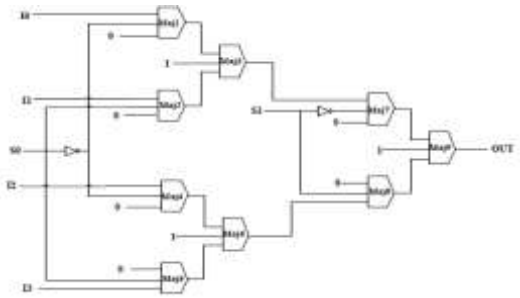


Fig.15. Schematic of 4:1 MUX

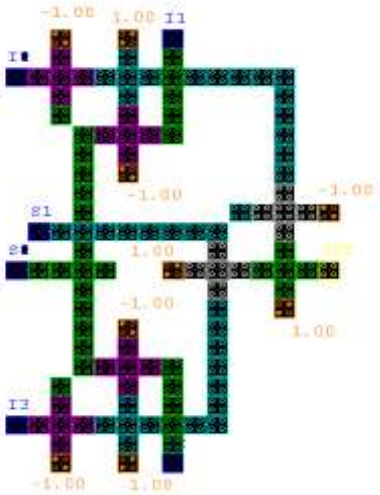


Fig.16. QCA Layout of proposed 4:1 MUX

2. Design Of 1 Bit Parallel Memory Using Proposed 2:1 Mux

The parallel memory cell is a fundamental and commonly used module in several digital circuits. Parallel memory enables us to access all the bits of the data word concurrently with low latency because it consists of several 1-bit memory loops. The drawback of the parallel memory is that for higher order memory, a lot of circuitry is repeated, so complexity and area of the circuits are increased considerably.Due to this, parallel memories are not chosen where the compact circuit is required. So any optimization in its complexity and area is appreciated. In paper**[**19] memory is designed using four dot 1 QCA, but simulation result is not reported in that paper, similarly, a parallel memory circuit presented in paper [20], designed using two dot 1 electron. Here the same approach is

used to design 1-bit parallel memory which comprises of two AND Gates and one 2:1 MUX and to meet the area challenge; the parallel memory is designed by using the 2nd proposed 2:1 MUX and its block diagram are represented in Fig. 17.

From the block diagram, it can be seen that two input signals control the operation of this memory chip. One input signal (Chip Sel) is used for chip selection, it activates or deactivates the memory chip and the

other input (Rd'/Wt) are used for selecting memory read, or memory write operation. The two inputs of 2:1 MUX act as data to be read or write in the memory. Whenever Chip Sel=0 memory is in reset mode, i.e., output=0. To perform a memory read or memory write operation, first of all, set Chip Sel=1. Now, for memory read operation set Rd'/Wt=0 then input I0 is selected. As it is connected to the output of MUX which is the previously stored value of the memory, so, in this case, the data to be read is available at the output. And for memory write operation set Rd'/Wt=1, so select line of the MUX will be 1 and input I1 will be selected. The data to be written is applied at the input I1, and therefore, the write operation is done in this case. The operation of the memory can be easily understood by its Functional table and truth table are shown in Table 3 and Table 4 respectively

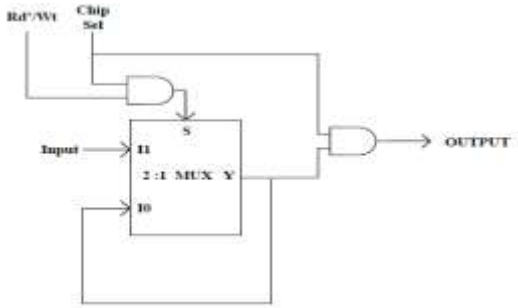


Fig.17. Bit |Parallel Memory

Table3. Functional table of Parallel memory

Chip Sel	Rd'/Wt	Memory operation
0	X	Reset
1	0	Memory read
1	1	Memory write

Table3. Truth table of Parallel memory

Chip Sel	Rd'/Wt	Input	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	previous output(0)
1	0	1	previous output(0)
1	1	0	Input(0)
1	1	1	Input(1)

The majority based block diagram of the parallel memory using proposed 2:1 MUX is shown in Fig. 18. The QCA layout requires five majority gates and one inverter as shown in Fig. 19. By using our proposed 2:1 multiplexer, the number of cells as well as the area occupied by the design is reduced, which shows its dominance over other designs.

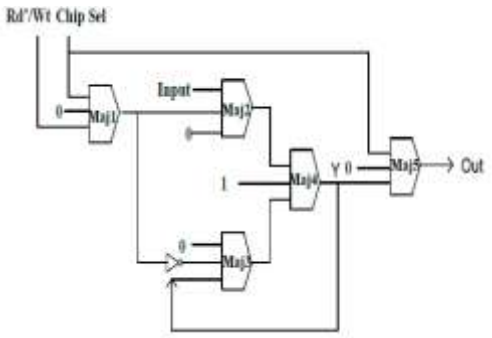


Fig.18. Schematic of |Parallel Memory

Majority based equation of this memory is shown in(8)

$$Out = M5(M4(M2(Input, M1(R_d / W_t, ChipSel, 0), 0), M3(M1, Y, 0), 1), 1), ChipSel, 0) \quad (8)$$

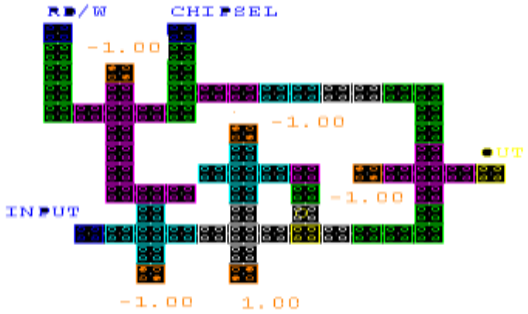


Fig.18.QCA layout of parallel memory

IV. Simulation Results And Discussion

For designing and simulation of the circuits, QCA Designer Ver. 2.0.3 is used using Bistable Approximation Engine with default parameters. Simulation results of 4:1 Multiplexer and parallel memory cell shown in fig.19and fig.20

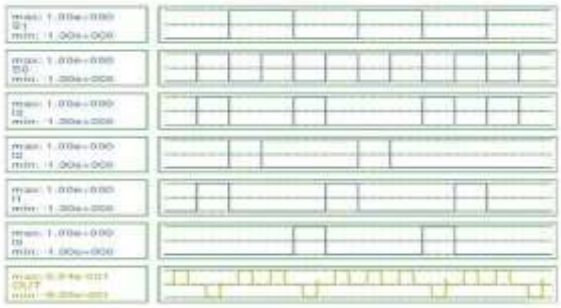
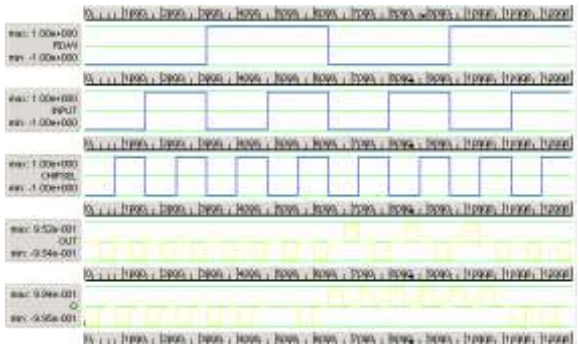


Fig.19. Simulation Results of 4:1 MUX



Simulation results 0f 1-bit parallel memory

Fig.20. Simulation results of one bit parallel memory

V. Conclusion

This paper proposes novel design approach of 2:1 MUX circuit using 4 Dot 2 Electron QCA. This approach has the capability to implement any higher order multiplexer and therefore using proposed 2:1 MUX, an efficient 4:1MUX is designed. Power dissipation analysis of the designed 4:1 MUX is done which is proclaiming the fact that the designed MUX is power efficient i.e. dissipating very less power, In order to demonstrate the utility of the proposed 2:1 MUX a 1- Bit Parallel Memory has been implemented. The proposed designs have shown significant improvements in comparison to the previously designed multiplexersin terms of area and complexity. Also, the circuit is having less delay than the other previous designs. Here robust coplanar

clock zone based crossover is used to construct the QCA circuits that result in a reduction of QCA cell count and area consumption without any latency overhead.

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